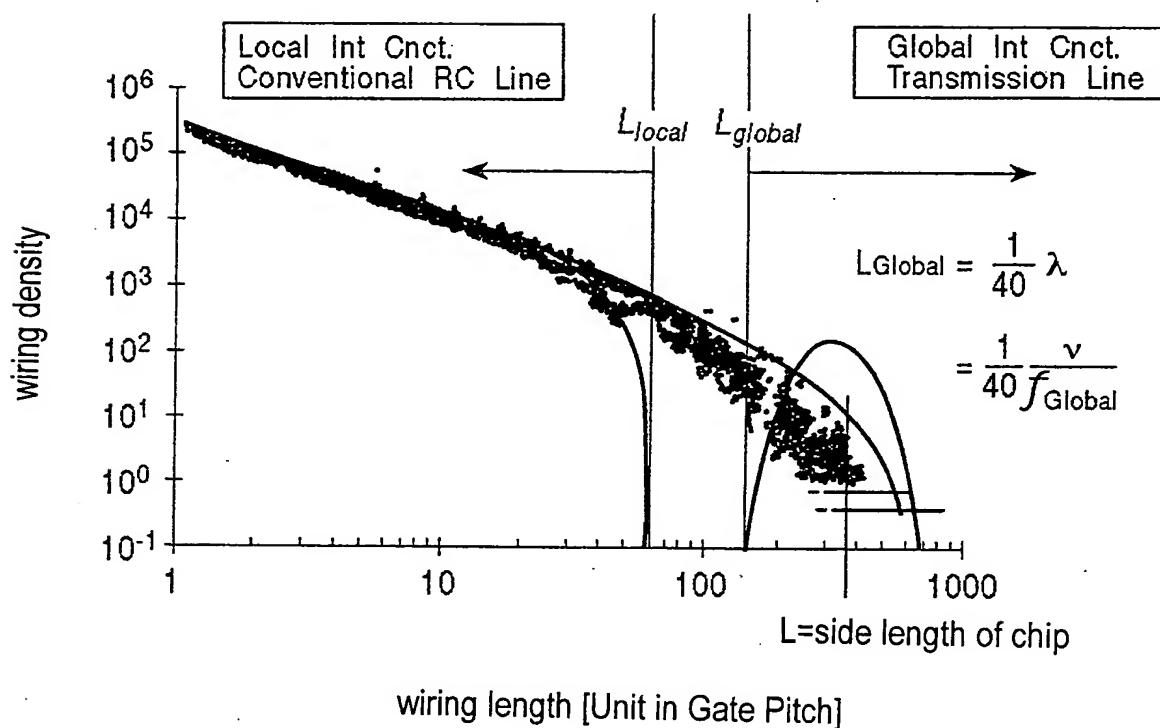


Fig. 1

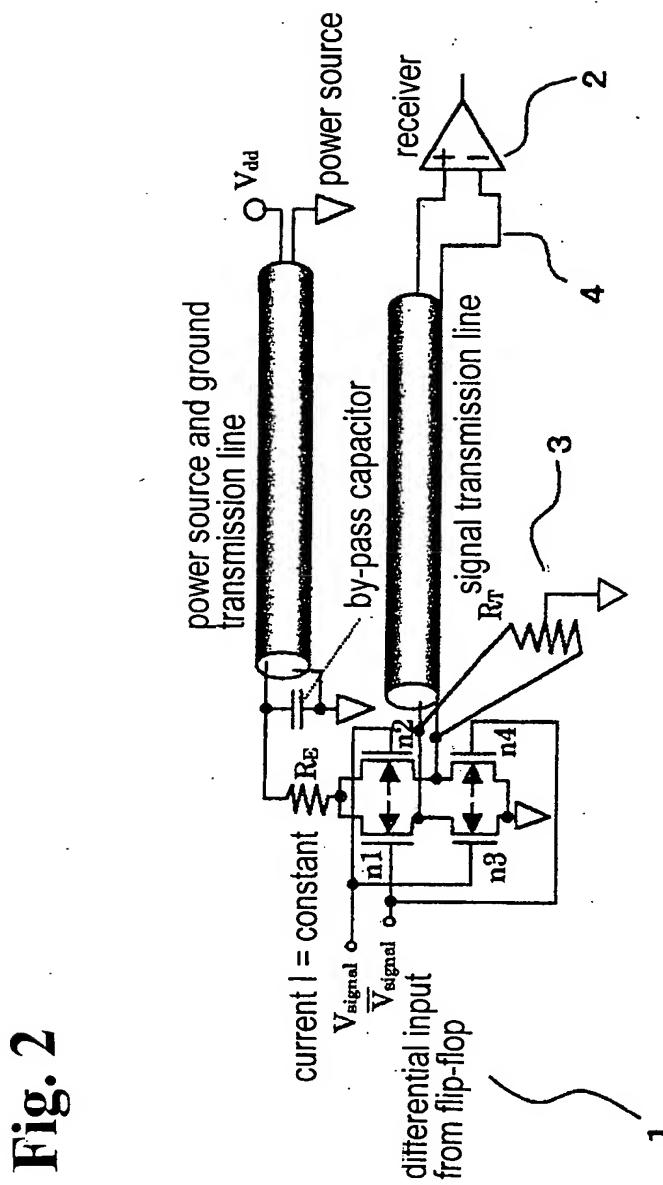


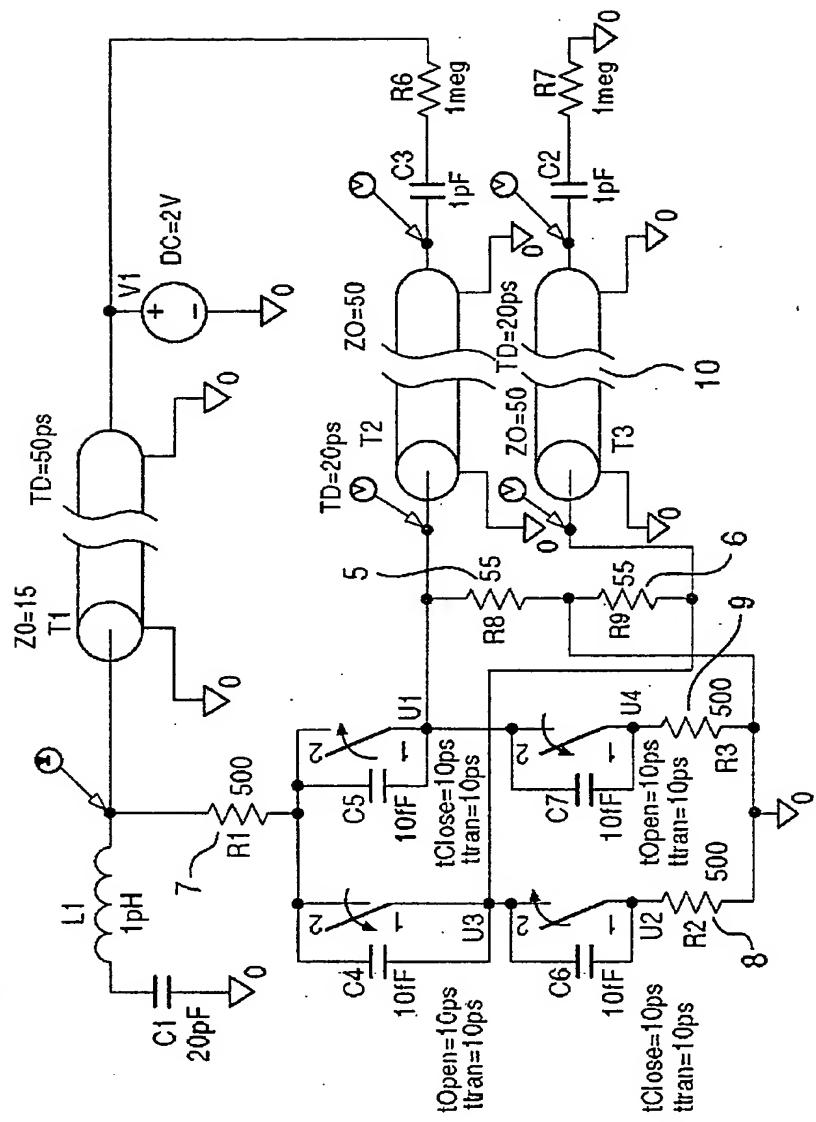
Fig. 3

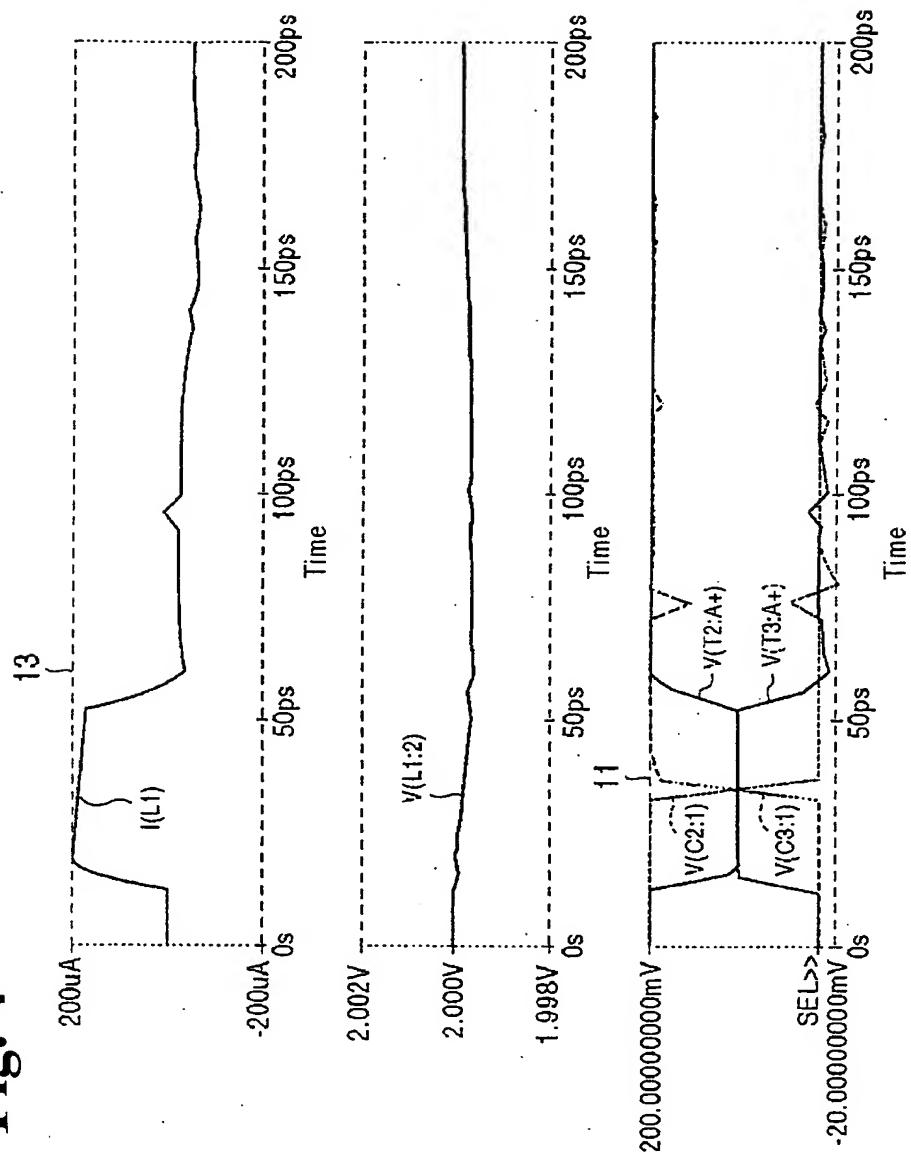
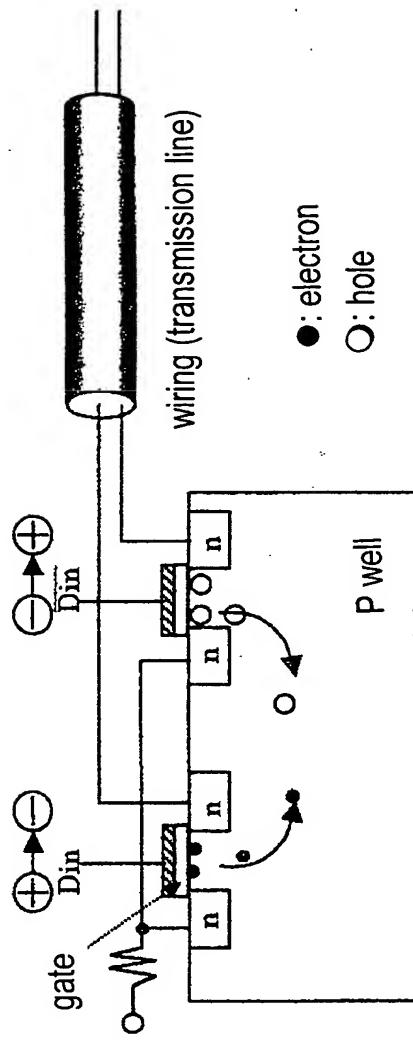
Fig. 4

Fig. 5



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Fig. 6

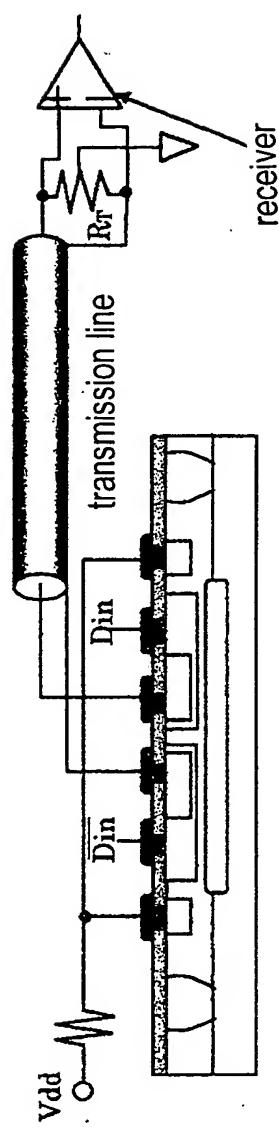
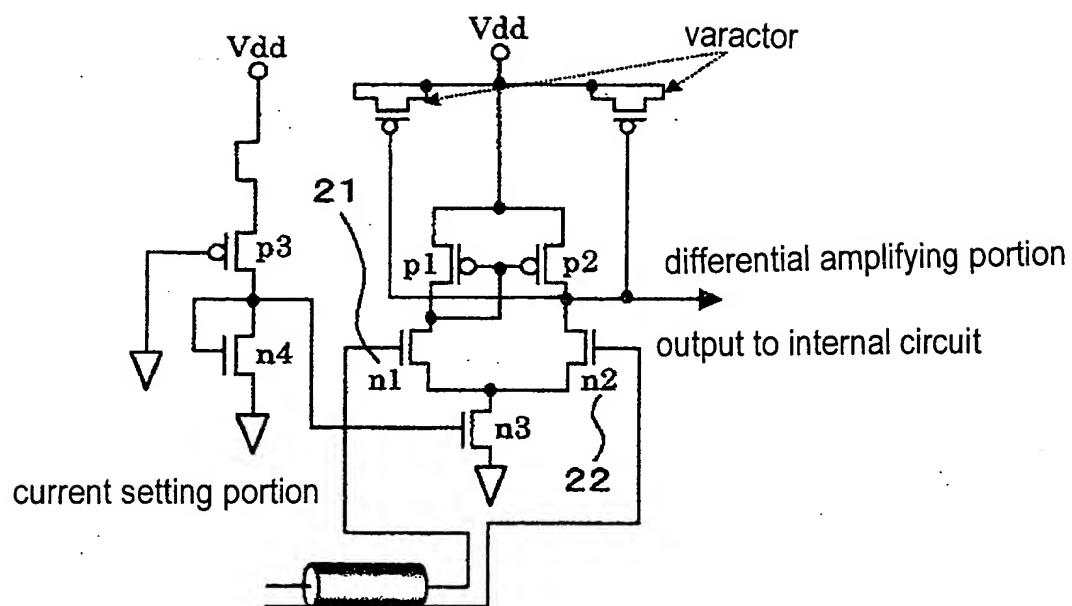


Fig. 7

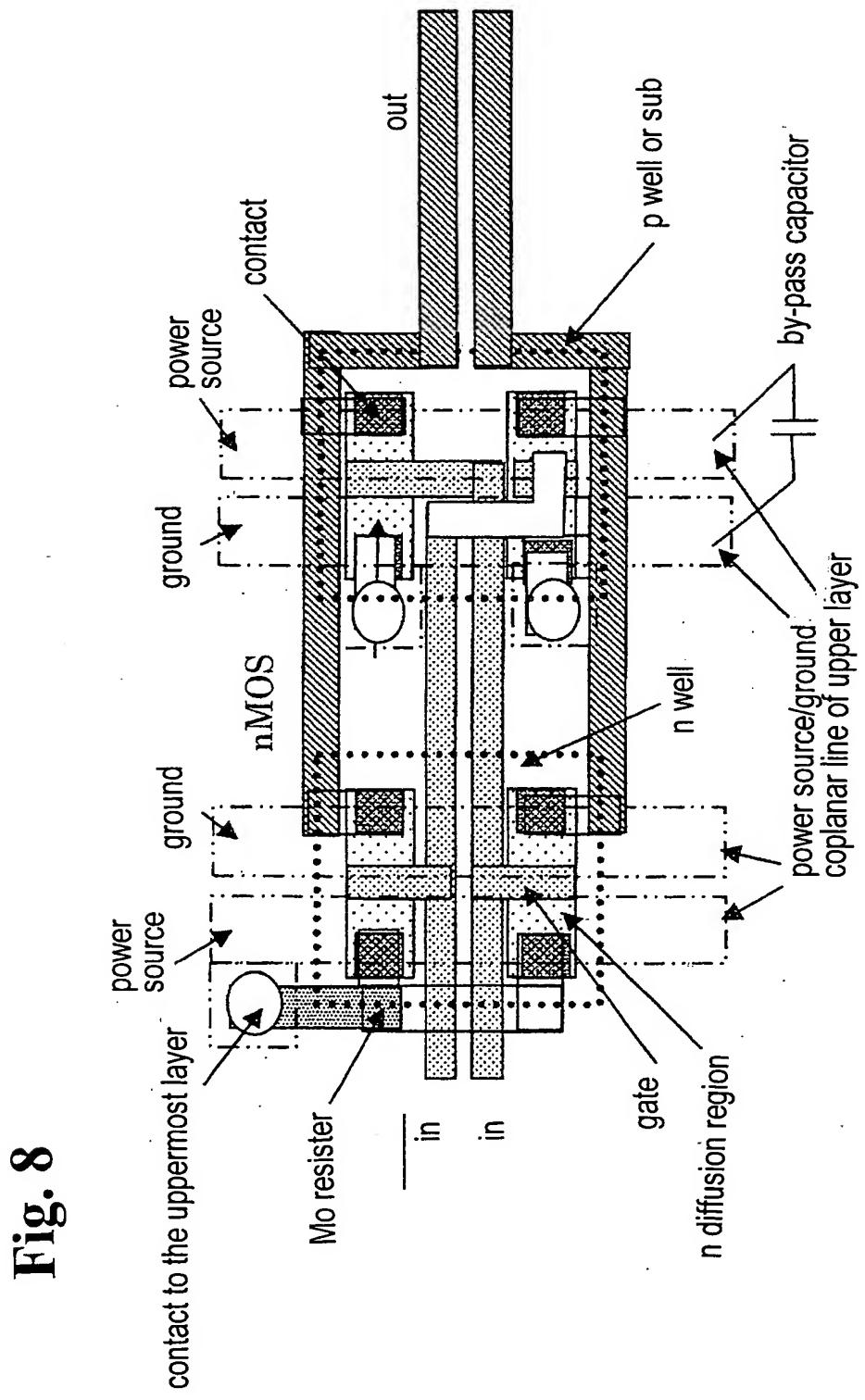


Fig. 8

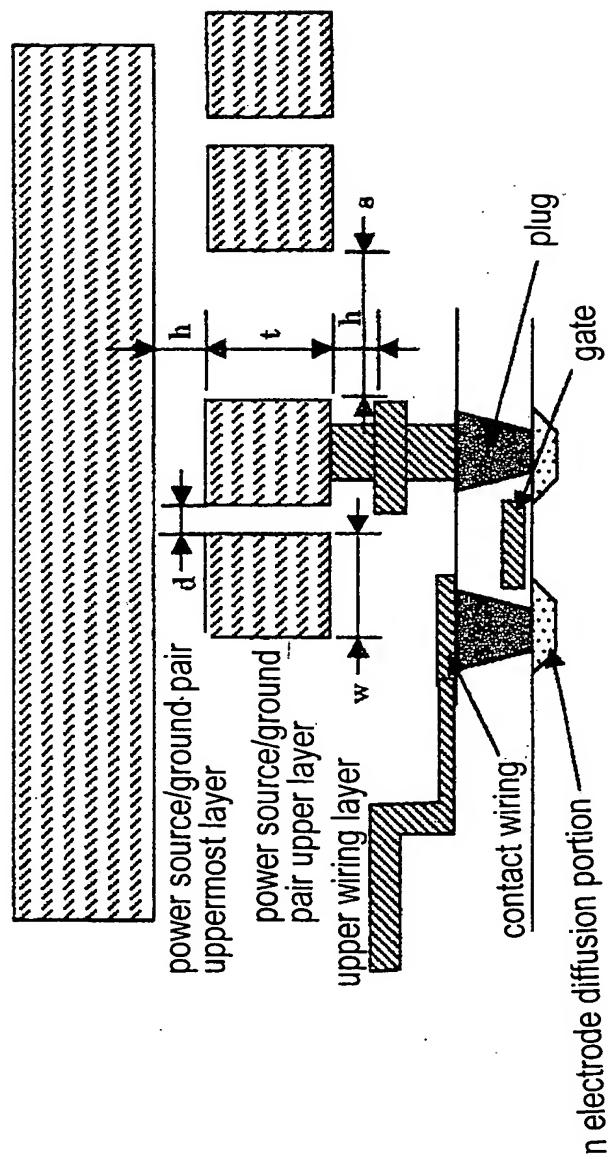
Fig. 9

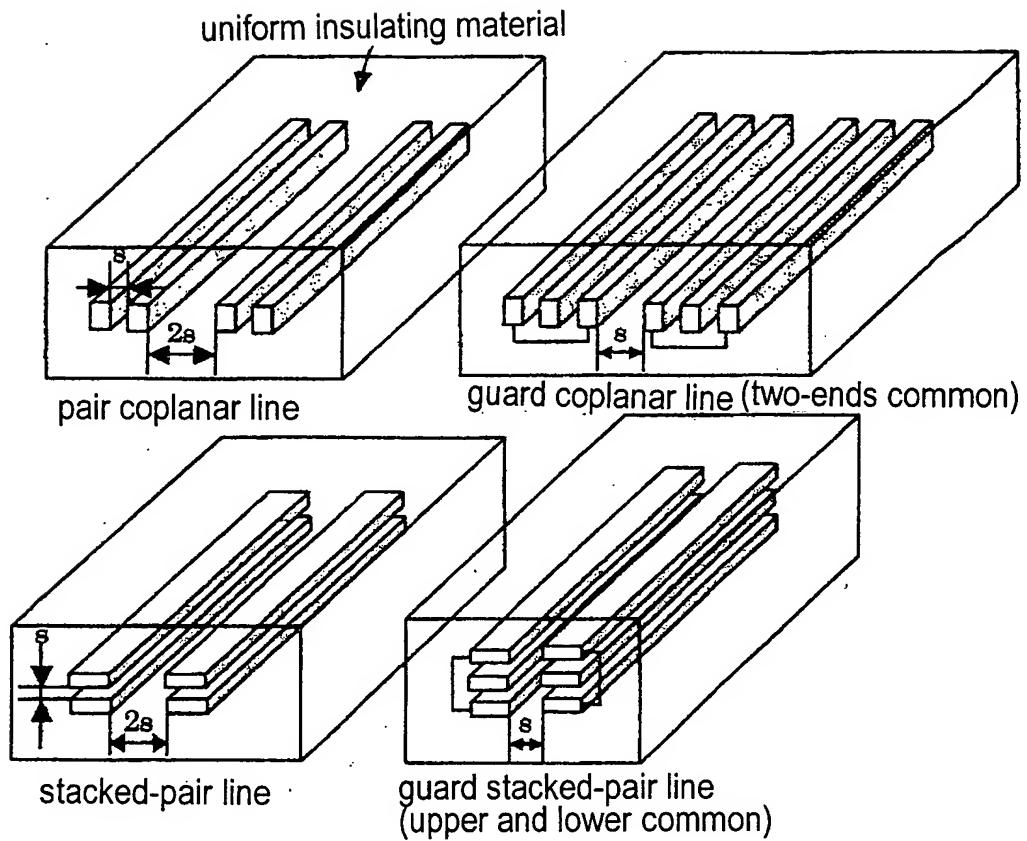
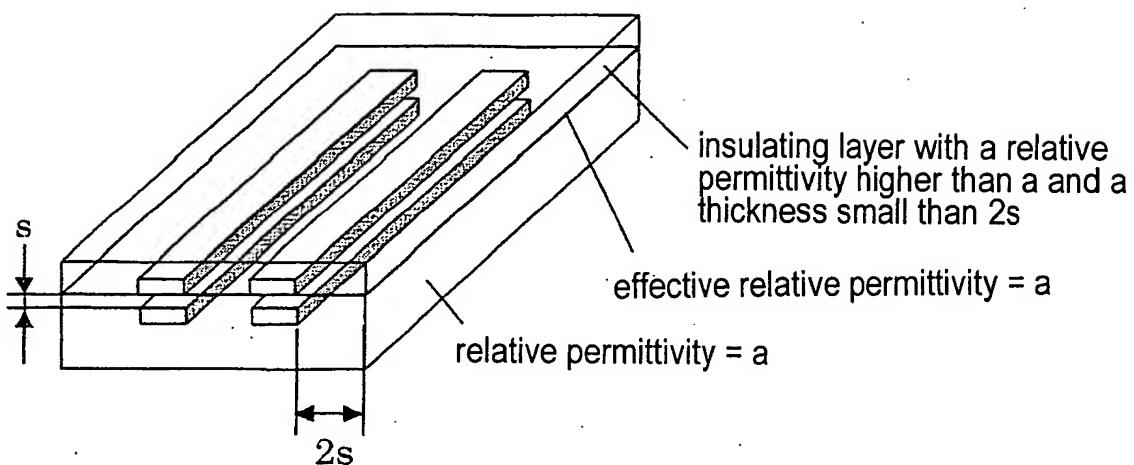
Fig. 10

Fig. 11

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Fig. 12(a)

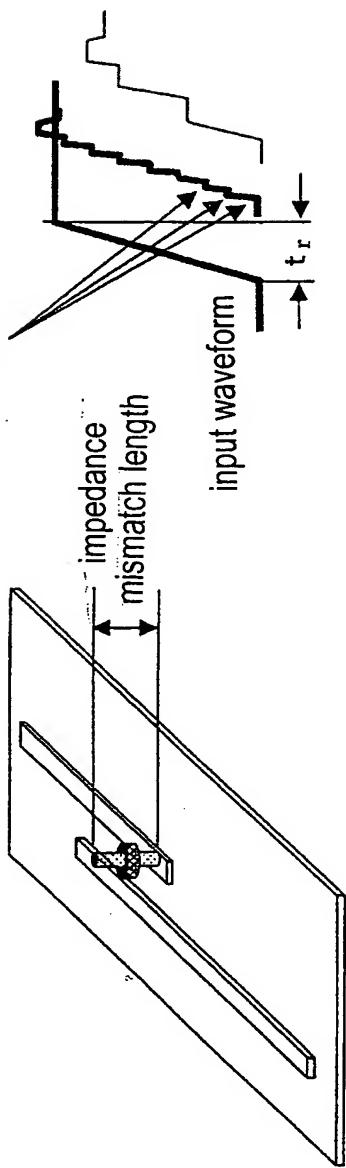
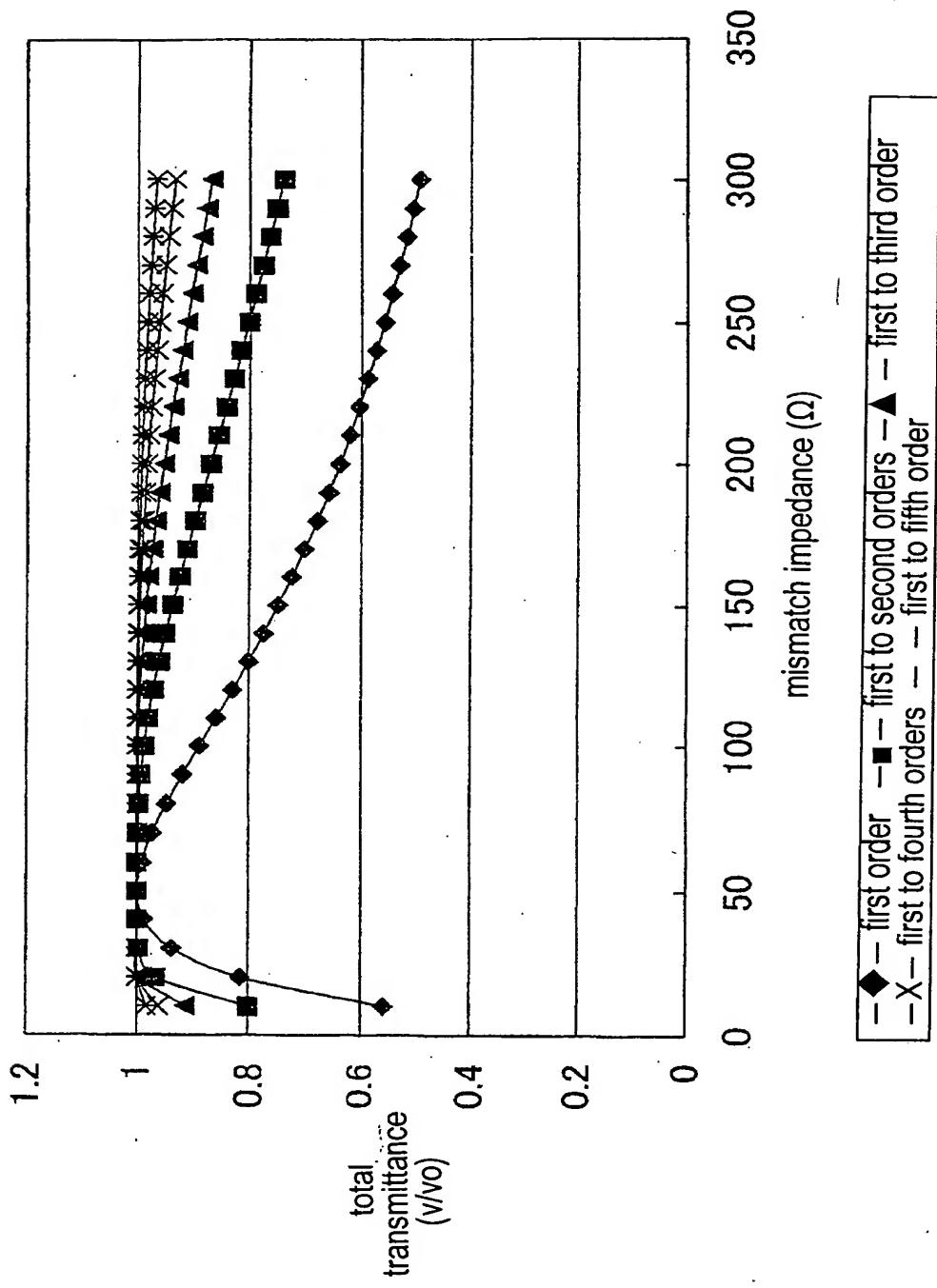


Fig. 12(b)

Fig. 13

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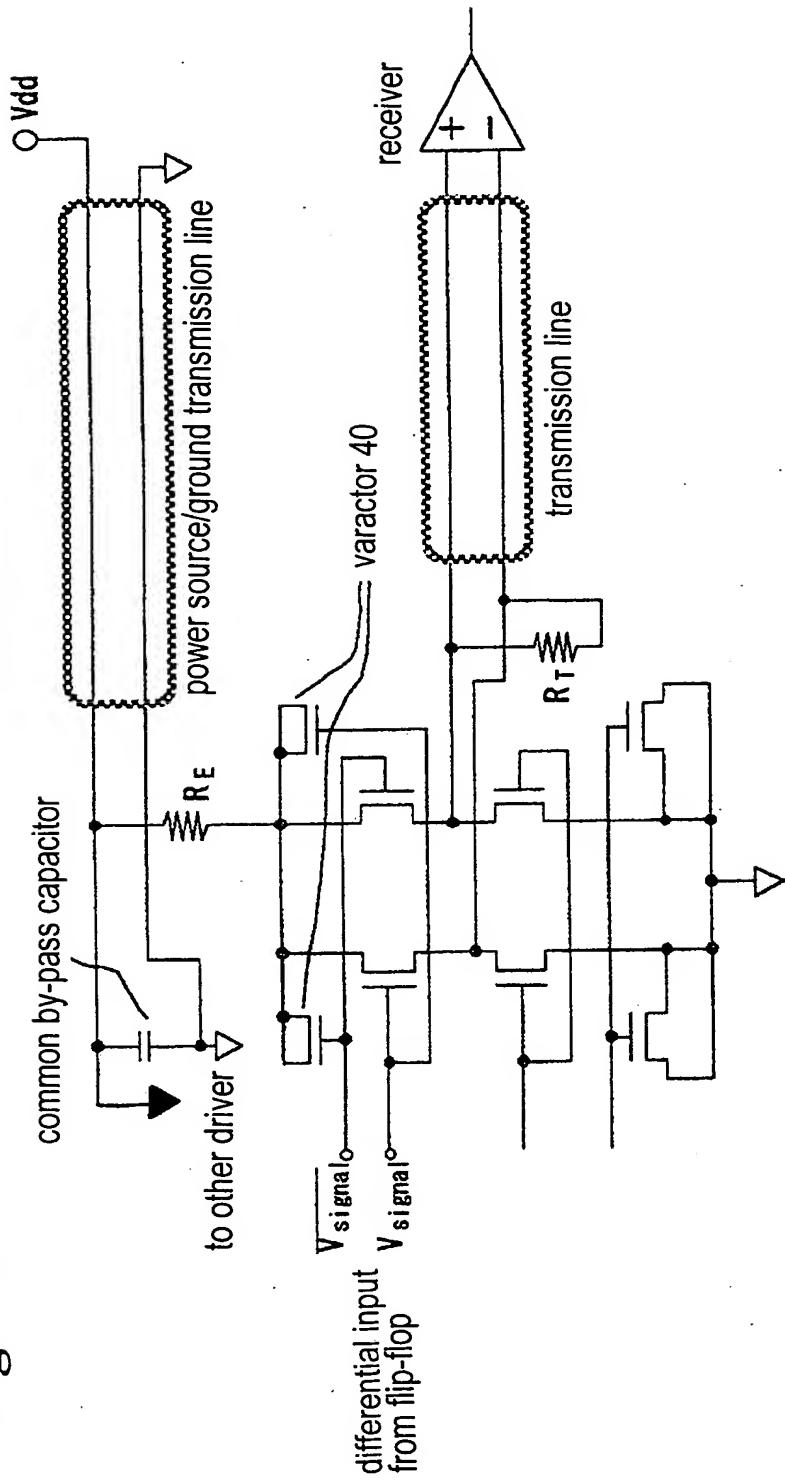
Fig. 14

Fig. 15(a)
plan view

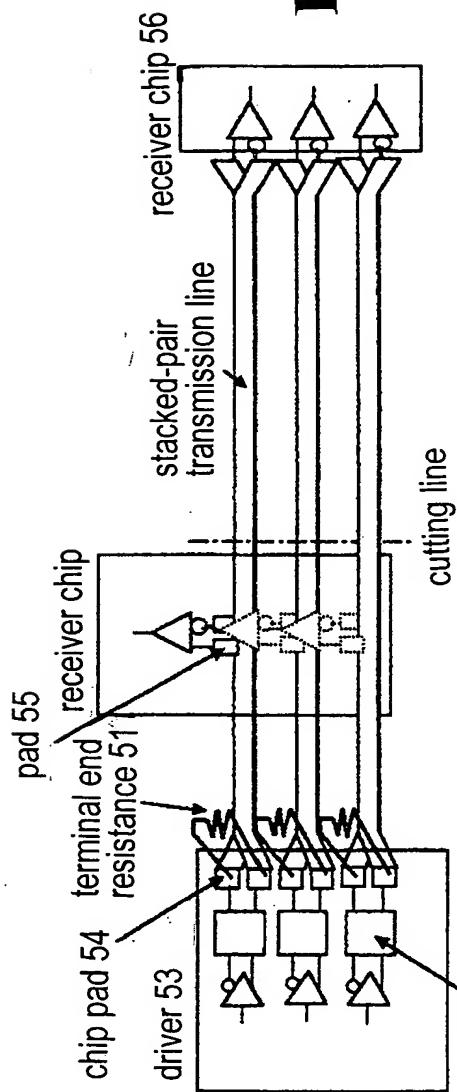
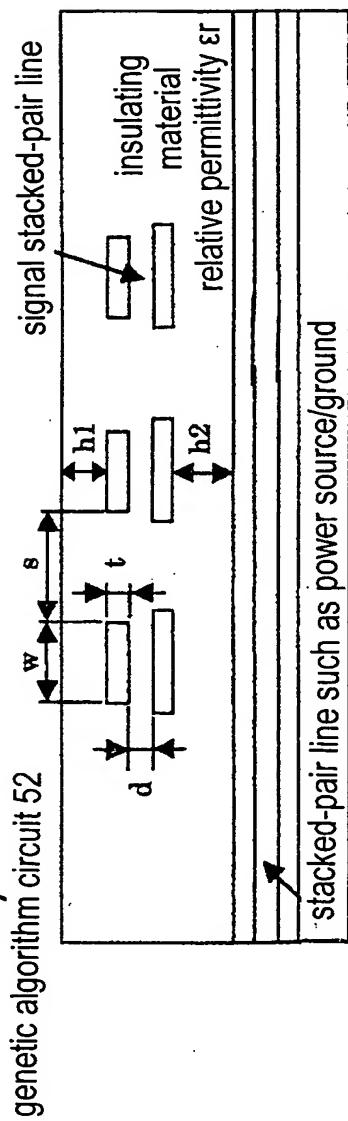


Fig. 15(b)
sectional view



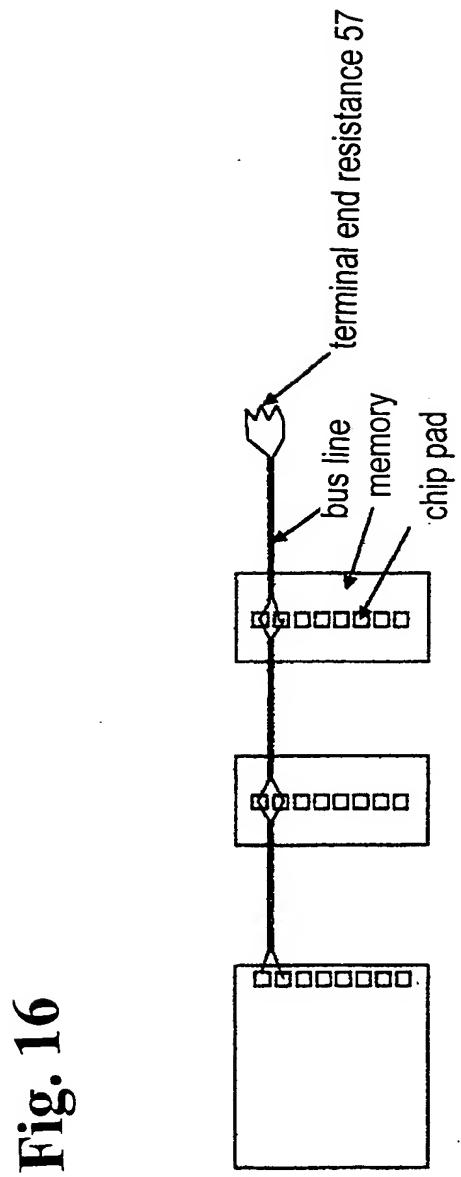


Fig. 16

Fig. 17

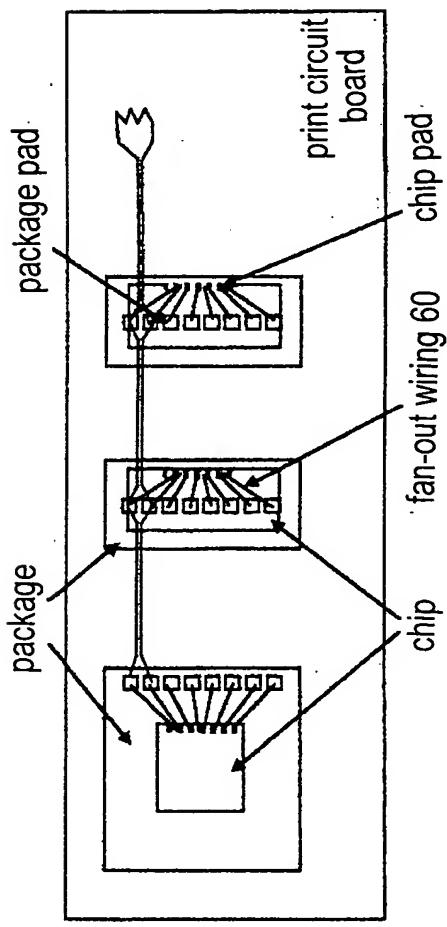


Fig. 18

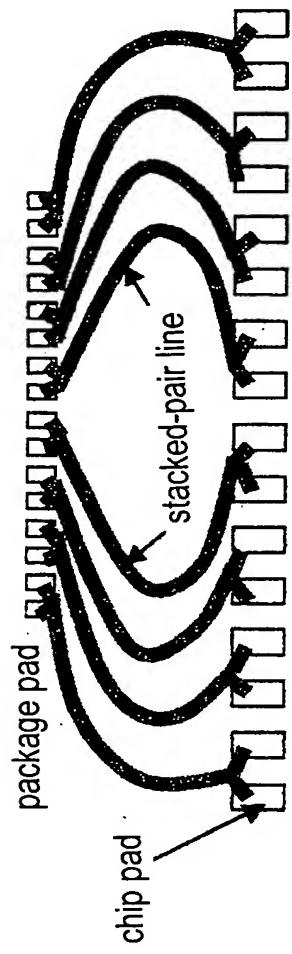


Fig. 19

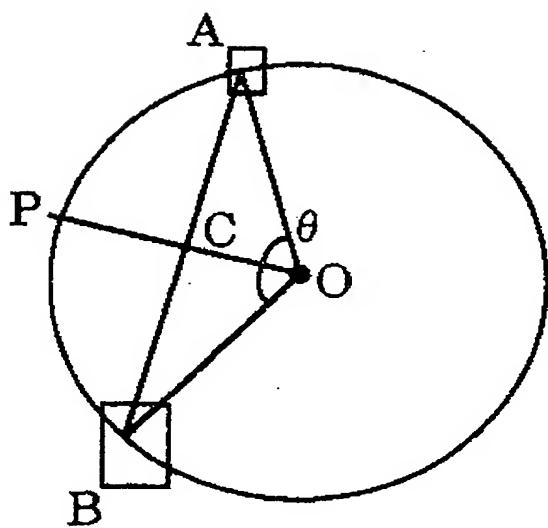


Fig. 20

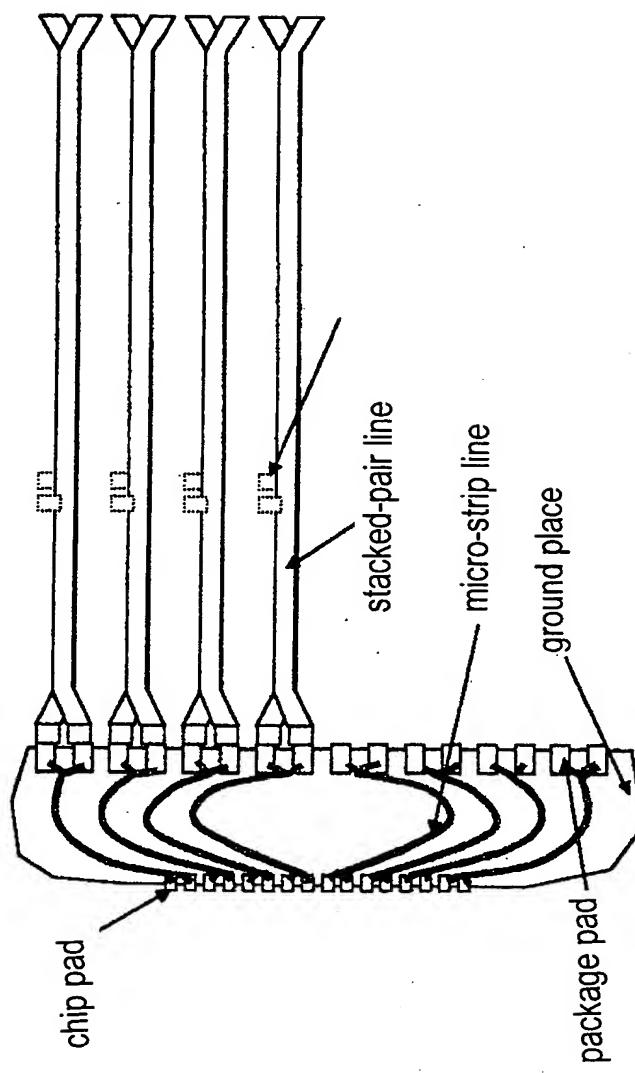


Fig. 21

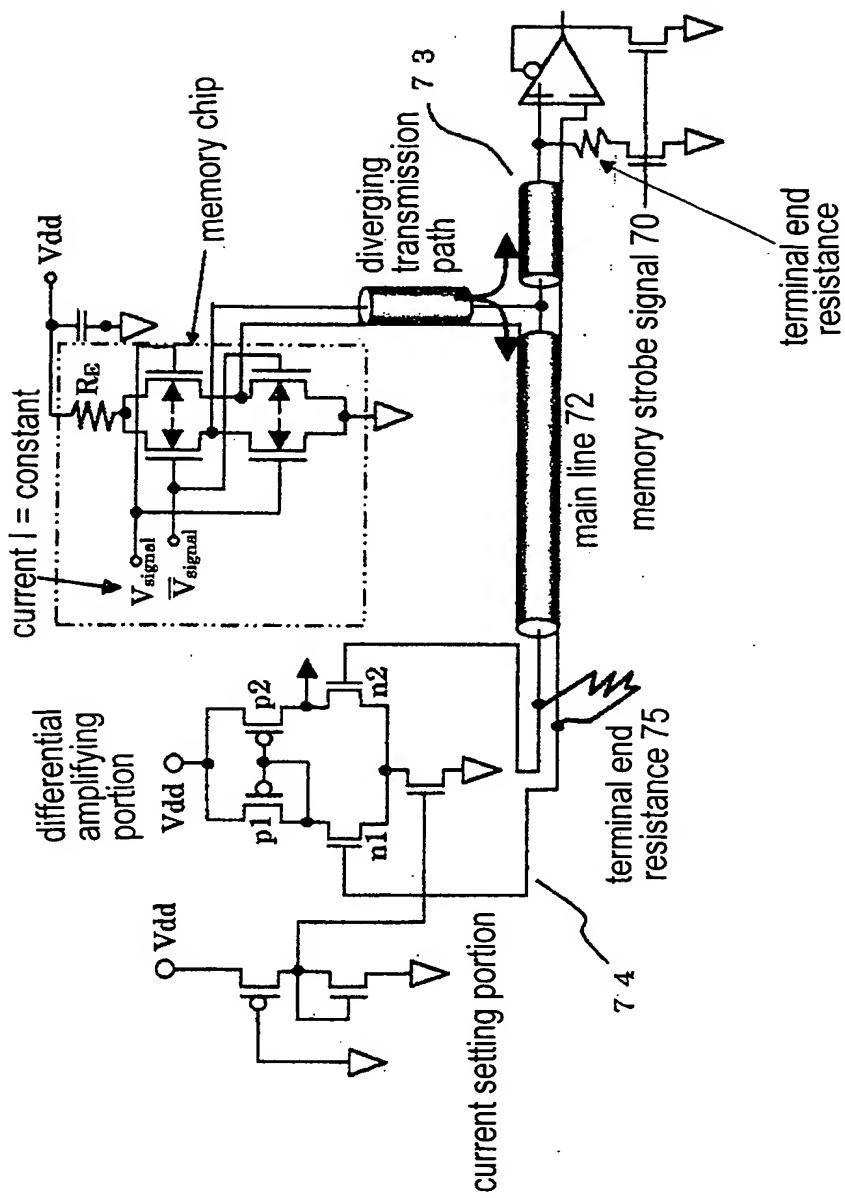


Fig. 22

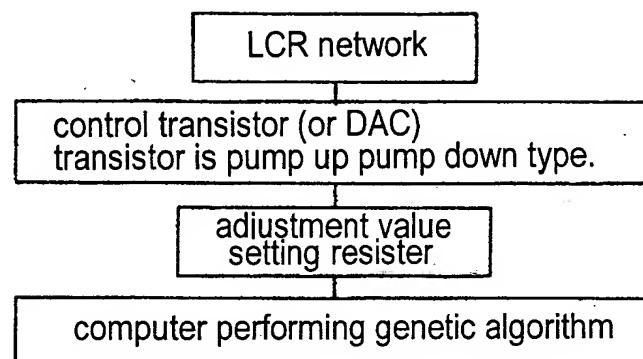
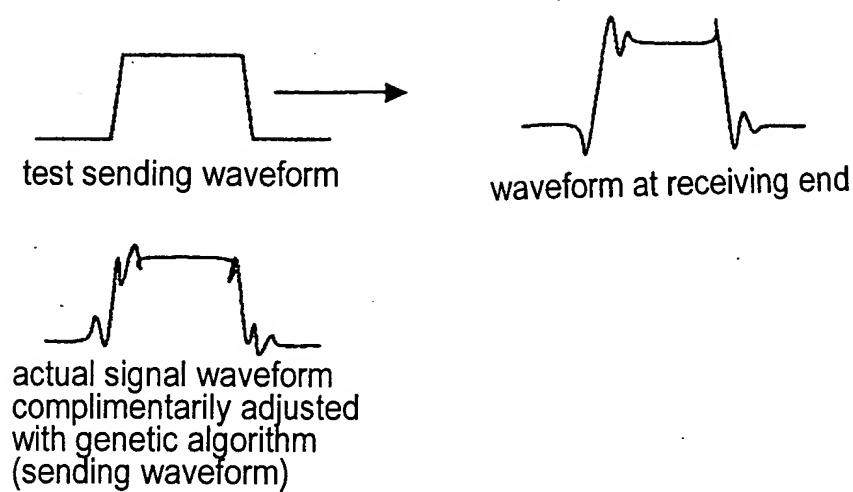


Fig. 23



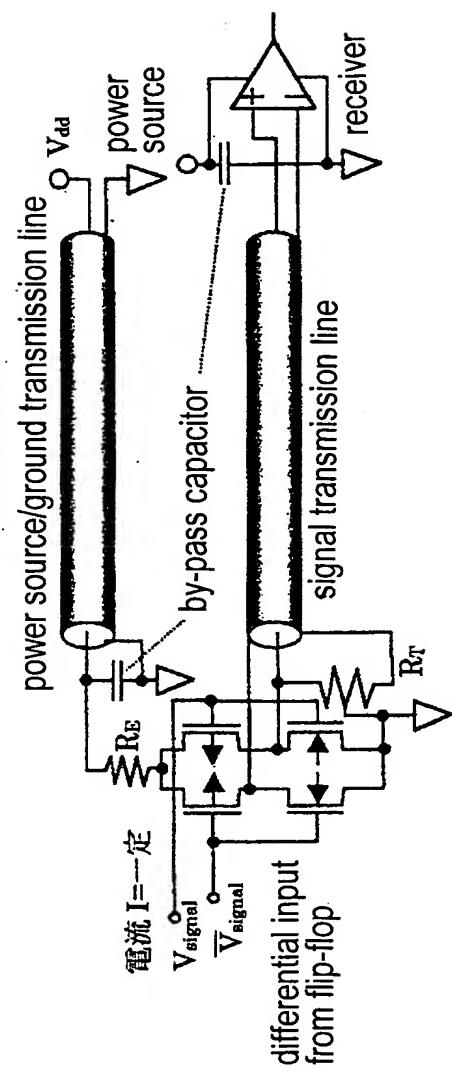


Fig. 24

Fig. 25

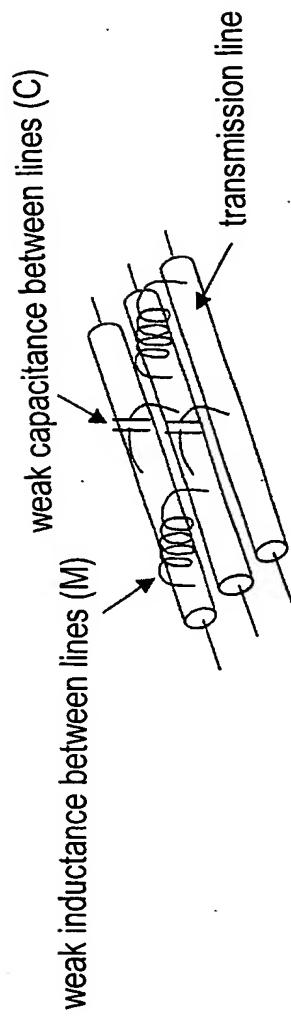


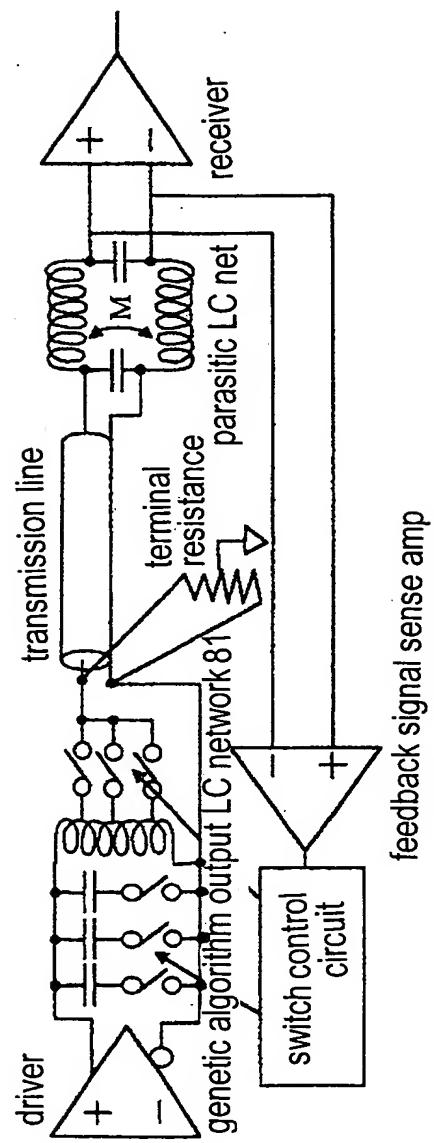
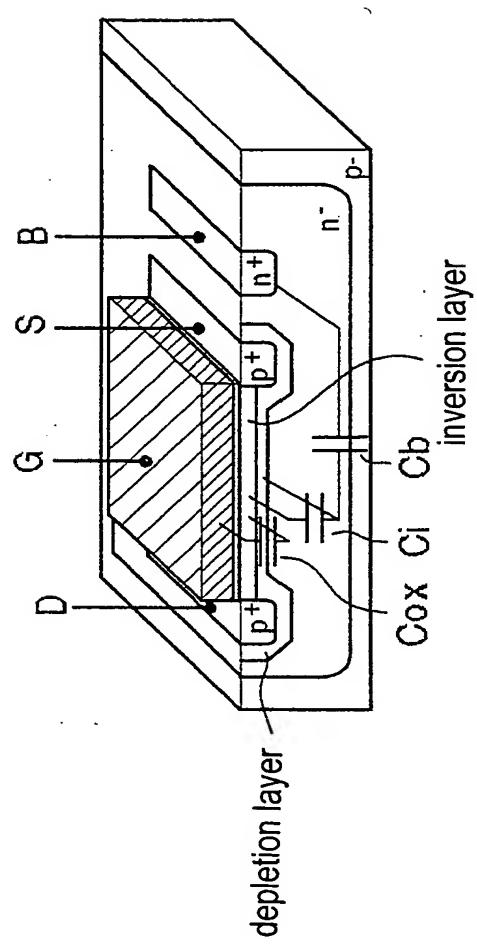
Fig. 26

Fig. 27

$1/C_{MOS} = 1/C_{ox} + 1/C_i + 1/C_b$
C_{ox}: capacitance of insulating layer
C_i: capacitance of depletion layer
under inversion layer
C_b: well capacitance

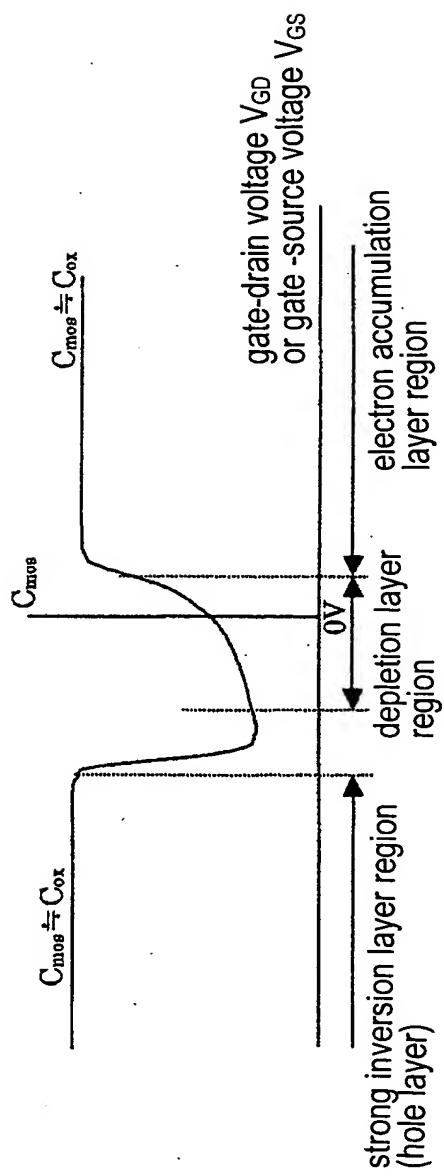
Fig. 28

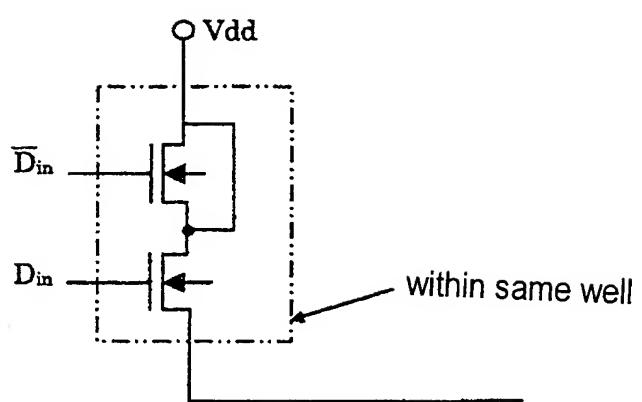
Fig. 29

Fig. 30

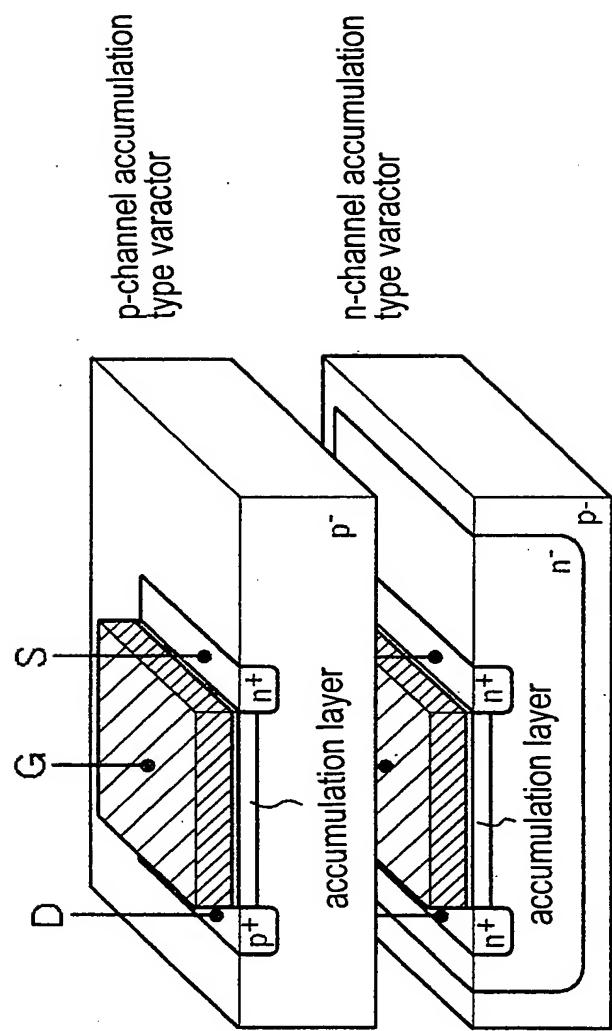
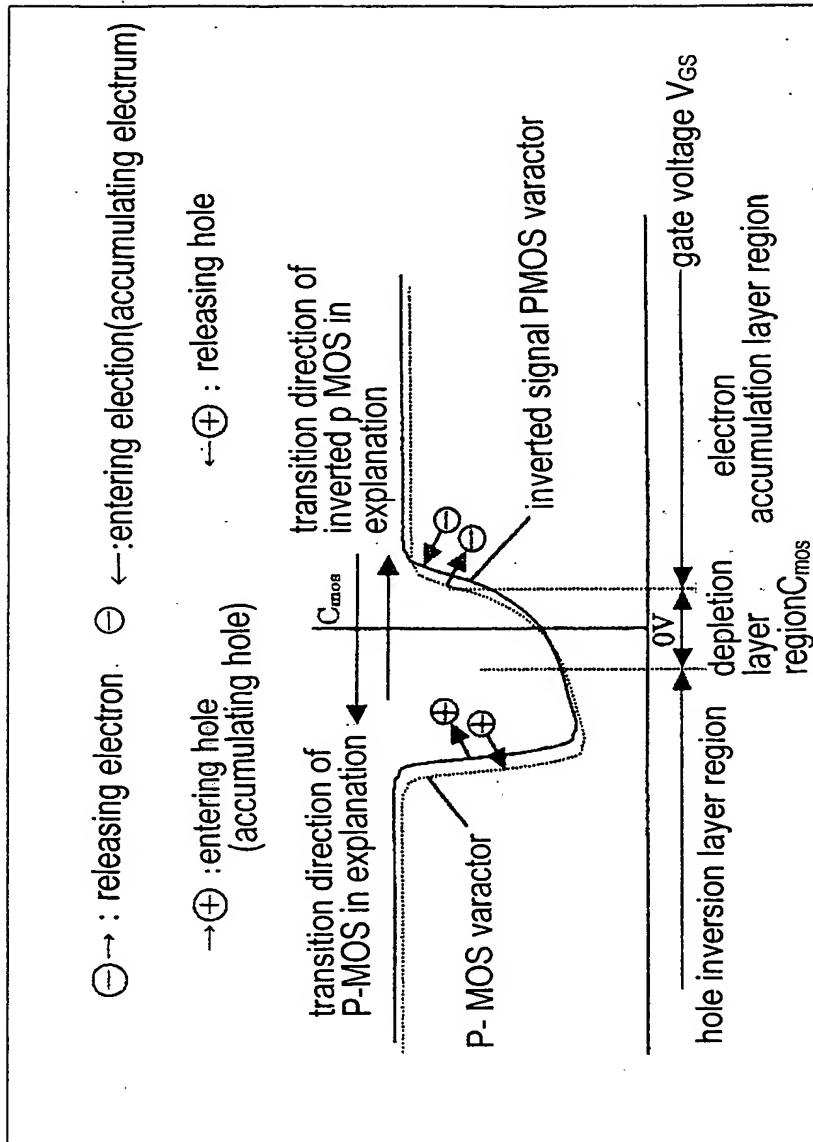


Fig. 31

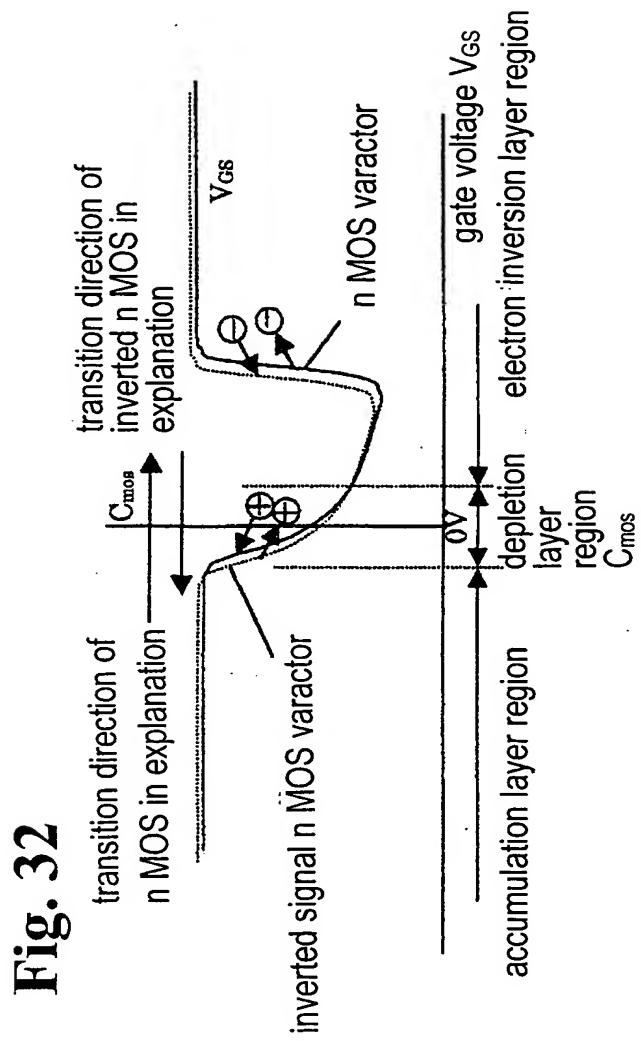


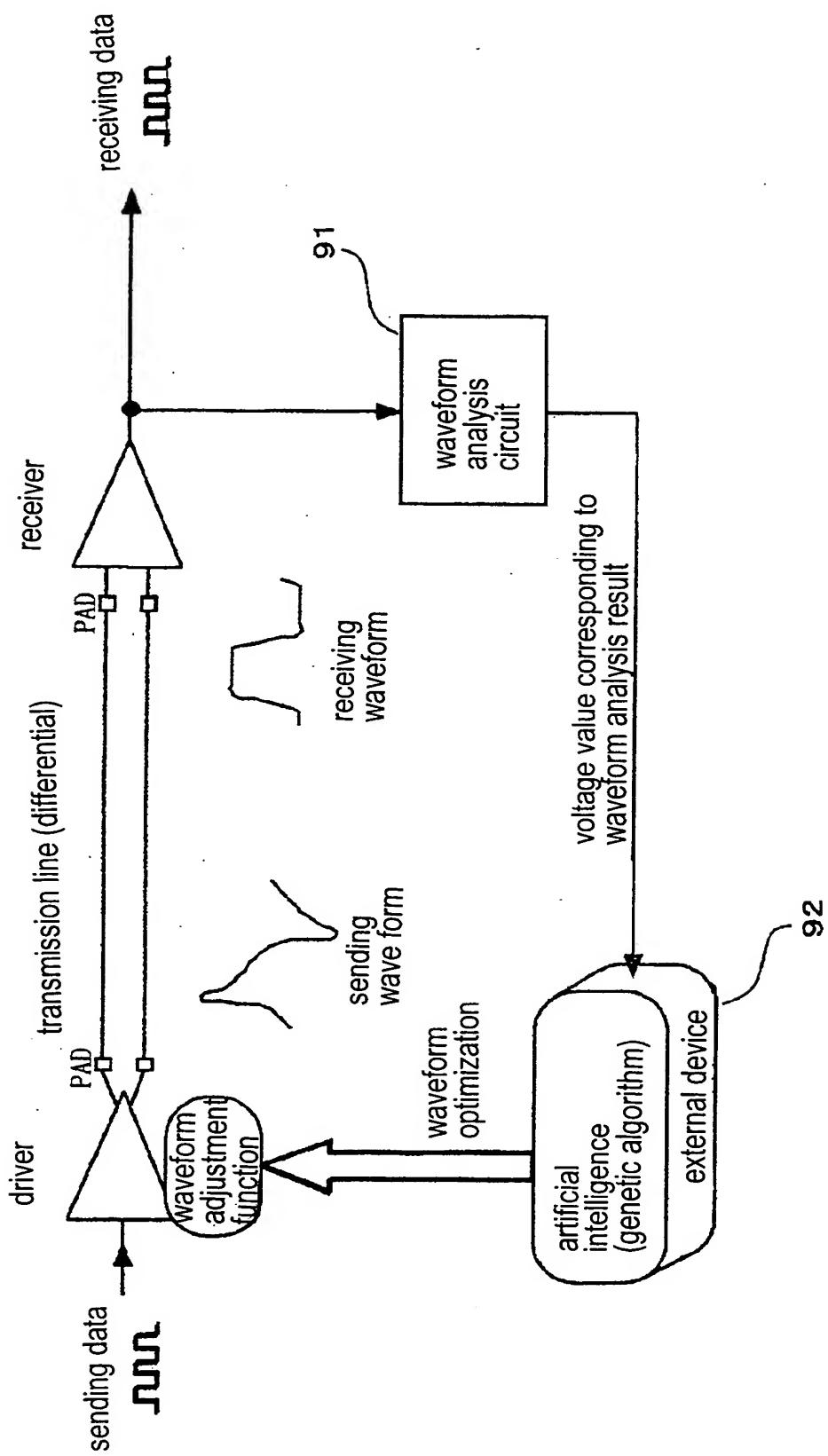
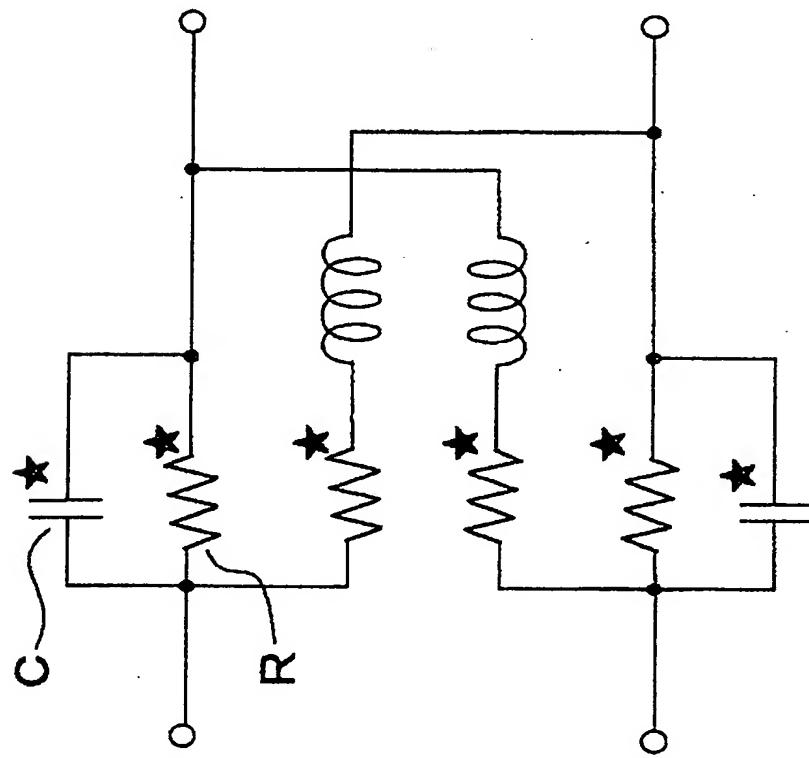
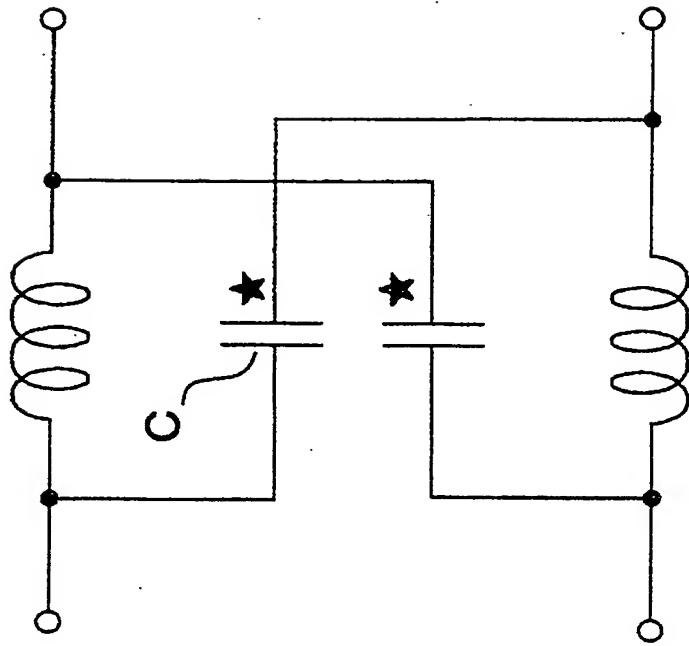
Fig. 33

Fig. 34(a)

(adjustment based on amplitude)

Fig. 34(b)★: variable value
(adjustment based on phase)

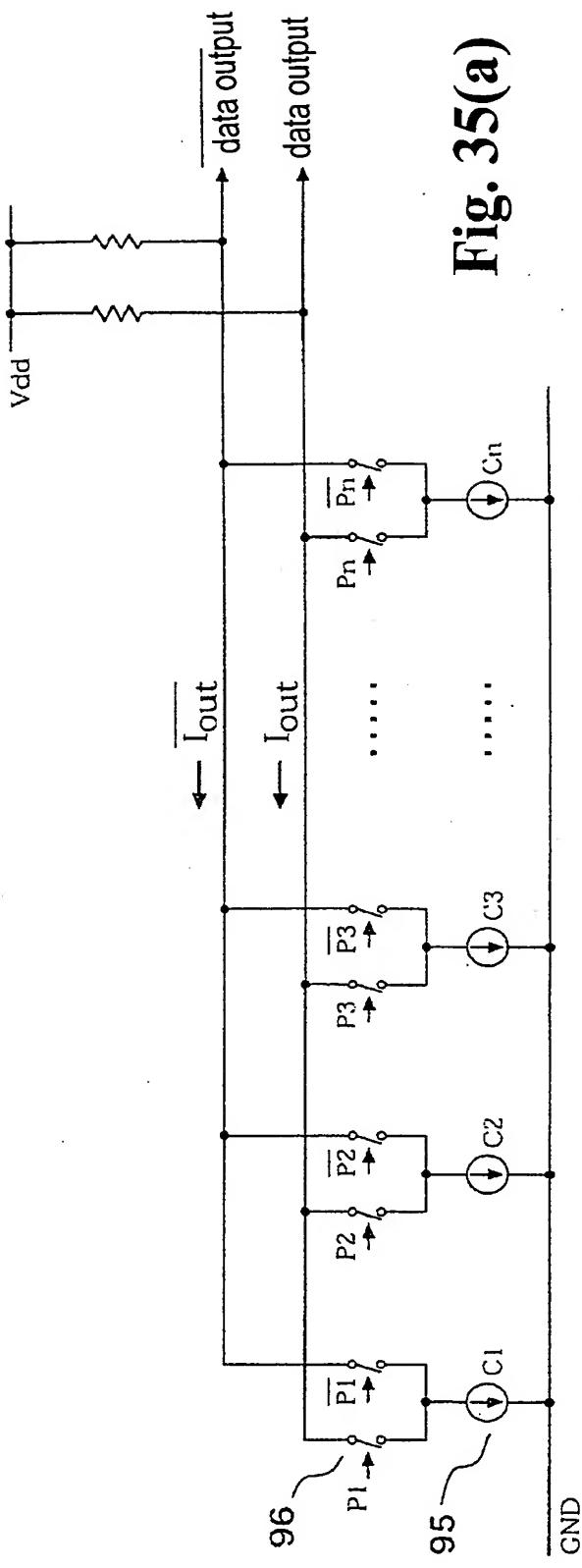


Fig. 35(a)

$C_0 \sim C_n$ are variable (externally adjusted) analog current values (direct current)

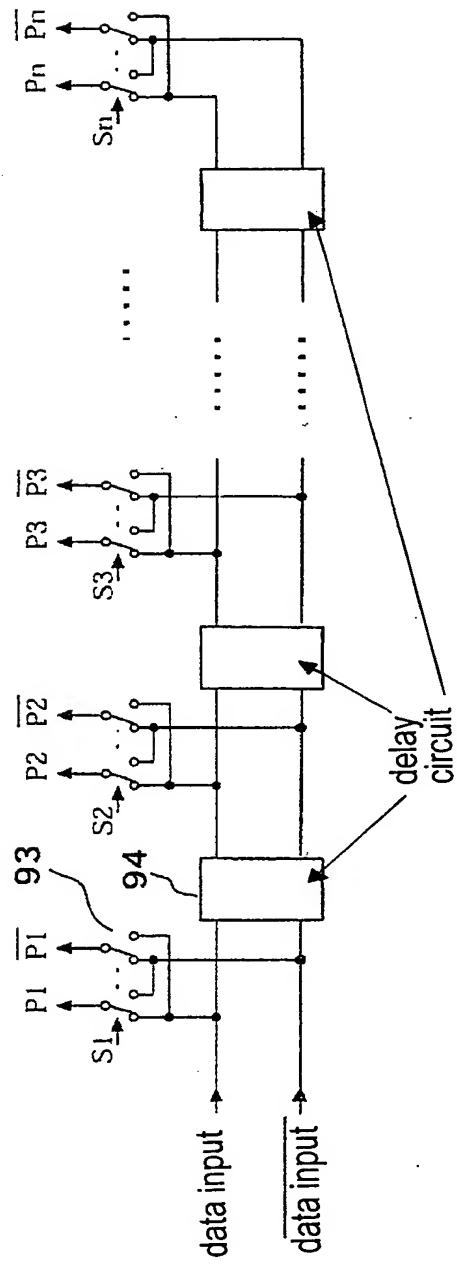
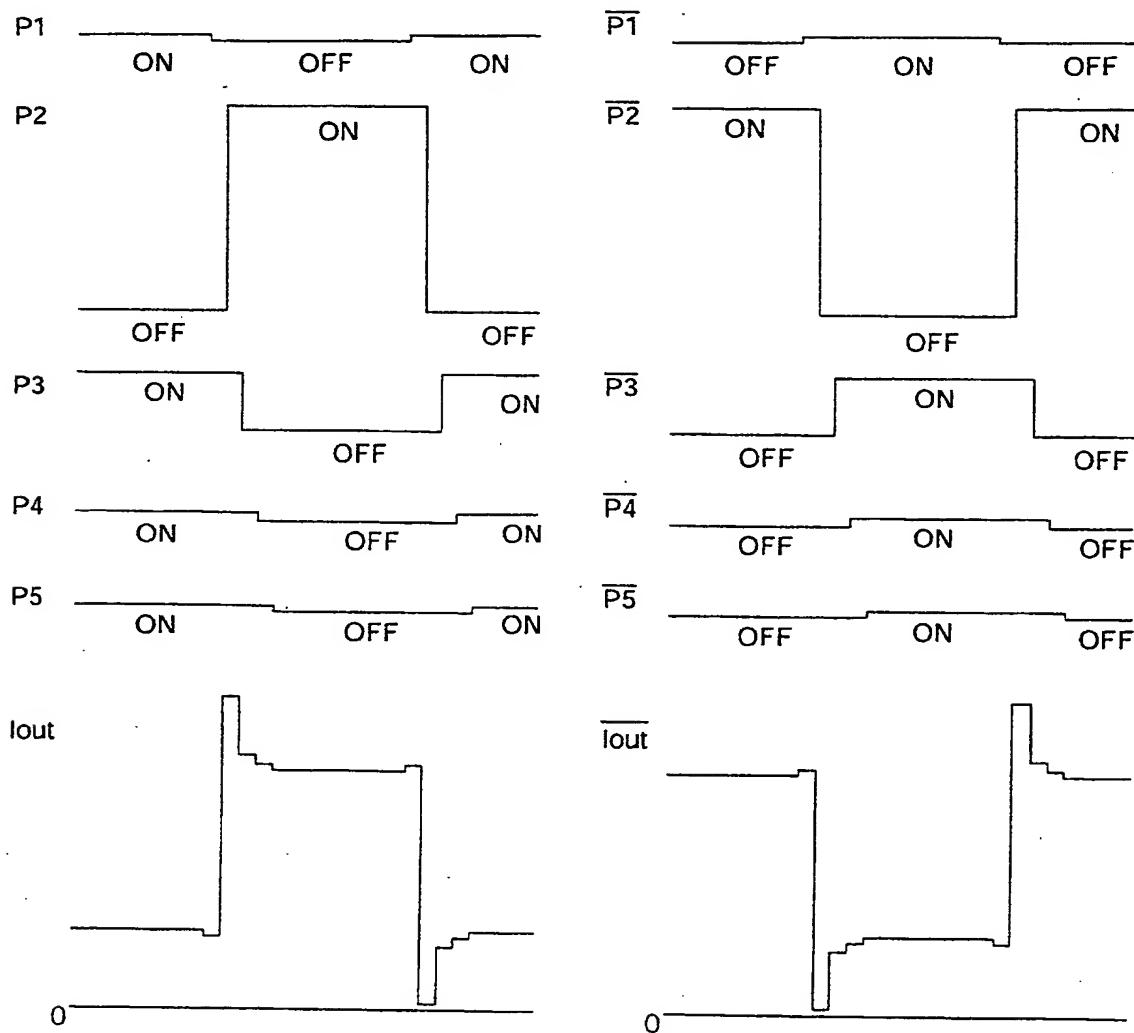


Fig. 35(b)

Fig. 36

waveform of I_{out} in which a current waveform of each switch and a corresponding current are combined:



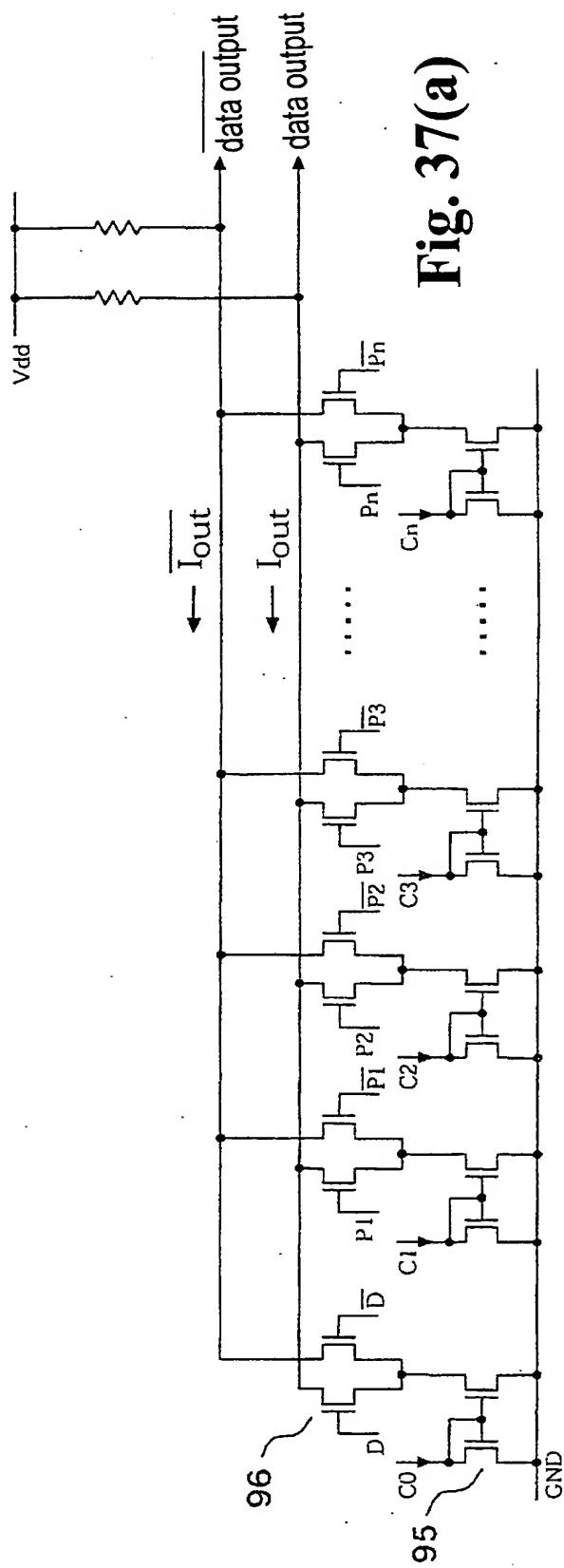


Fig. 37(a)

$C_0 \sim C_n$ are variable (externally adjusted) analog current values (direct current)

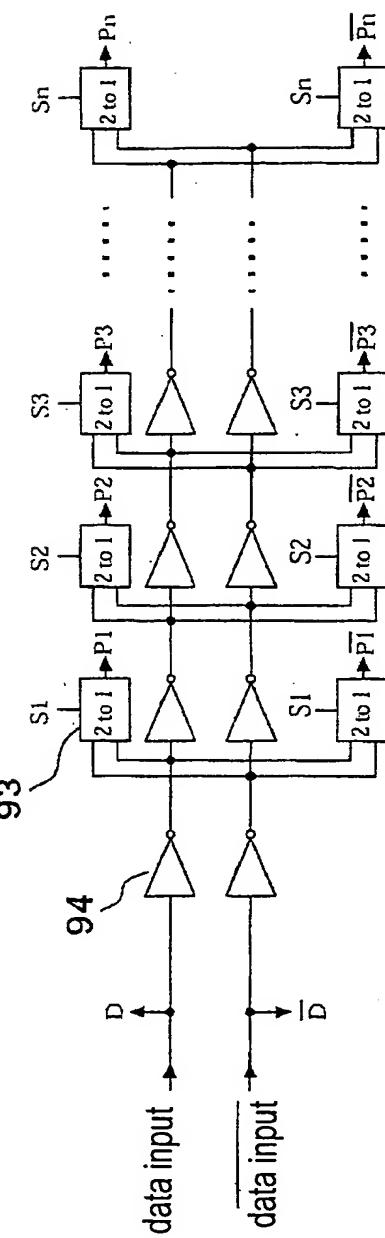
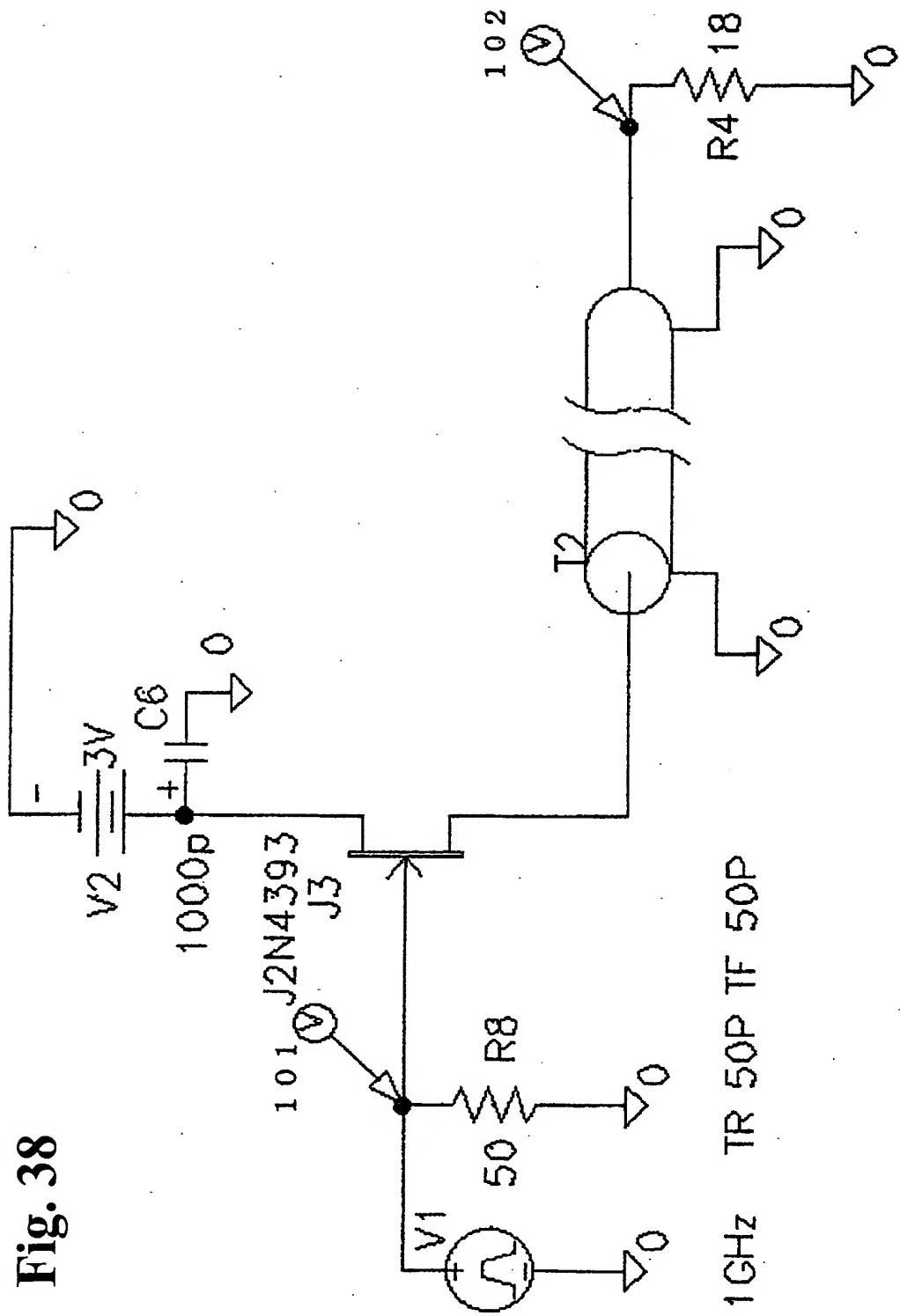


Fig. 37(b)

Fig. 38



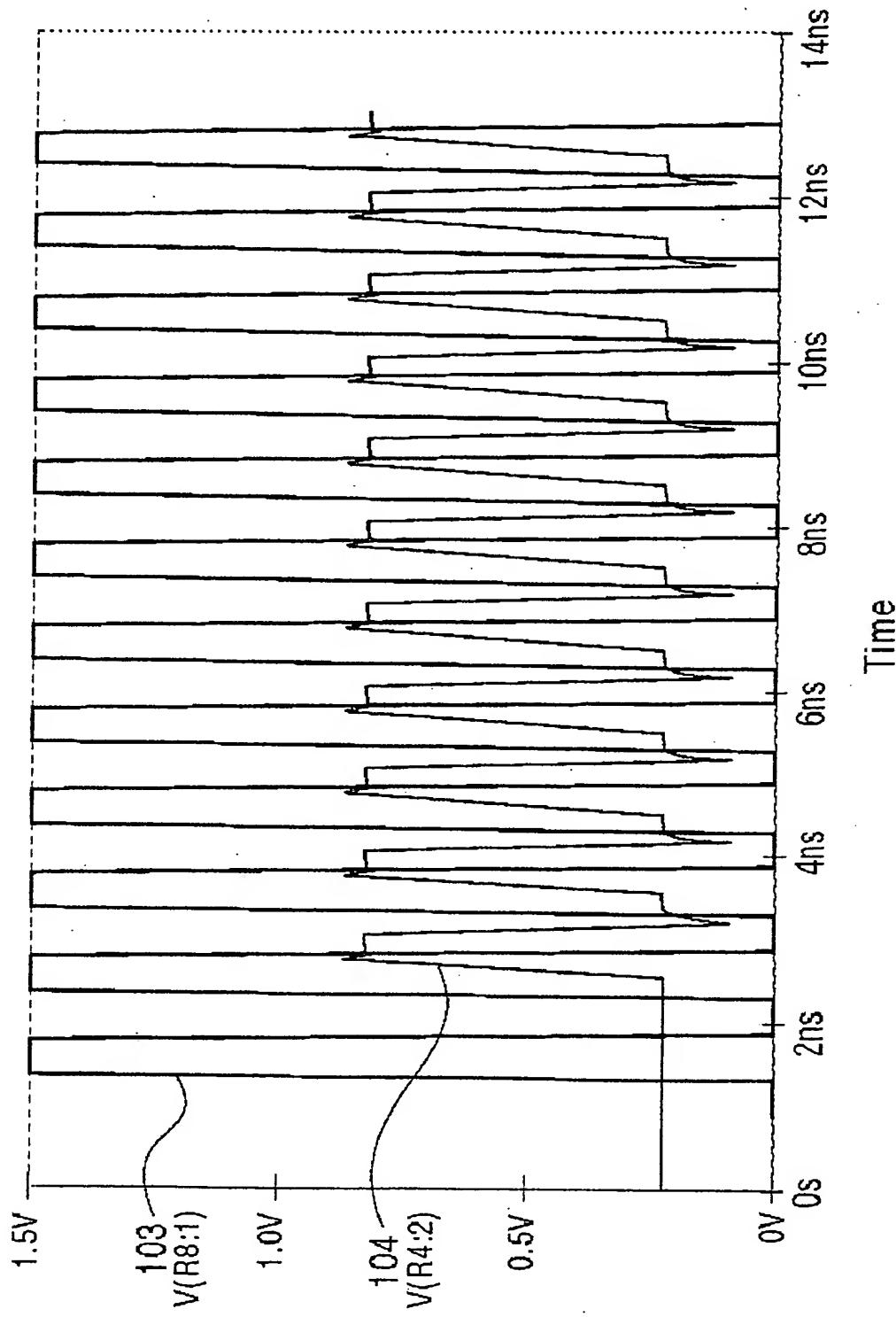


Fig. 39

Fig. 40

Data:C: # My_Documents # spara # MS_PL_FR4 # MS_1_1_2_1.S2P
 V:0
 I:0
 Data:C: # My_Documents # spara # MS_PL_BTREGIN # msbp11s21.s2p
 V:0
 I:0
 Data:C: # My_Documents # spara # aron # Ms11s21.s2p
 V:0
 I:0

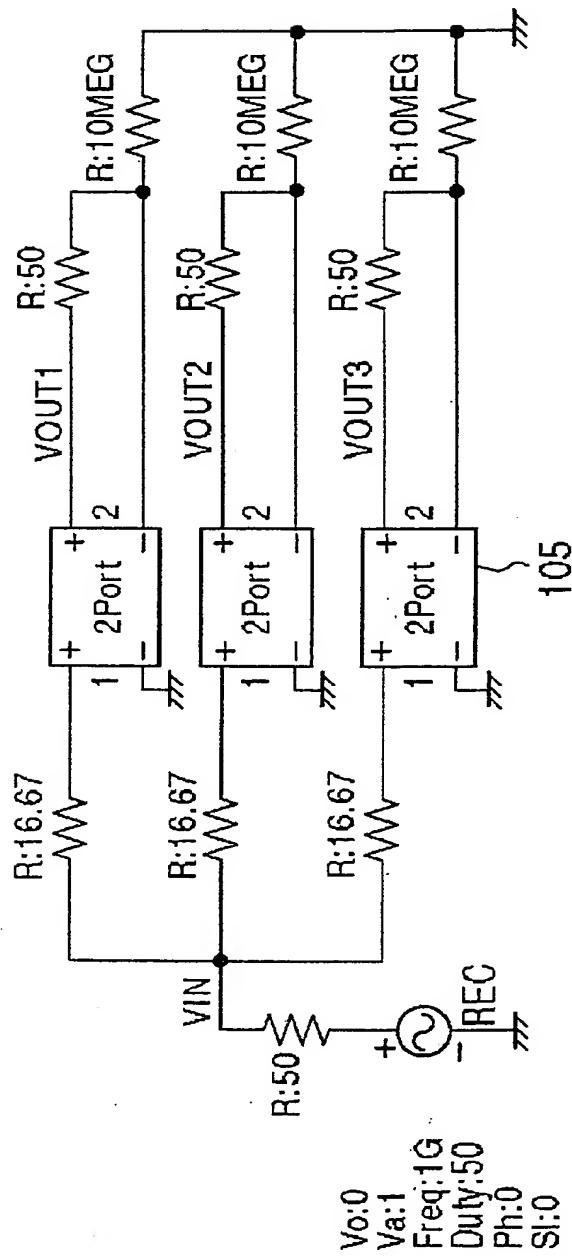
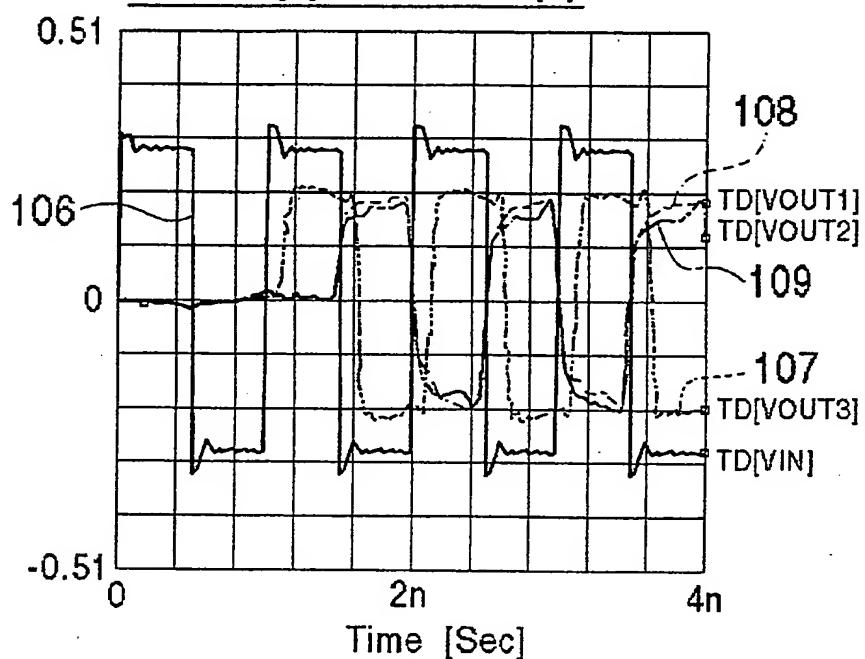


Fig. 41

Equ: TD[VOUT1]; TD[VOUT2]; TD[VOUT3]; TD[VIN]

Real/Ref: 0[U] Scale: 0.1002[U]



Equ: TD[VOUT1]; TD[VOUT2]; TD[VOUT3]; TD[VIN]

Real/Ref: 0[U] Scale: 0.1002[U]

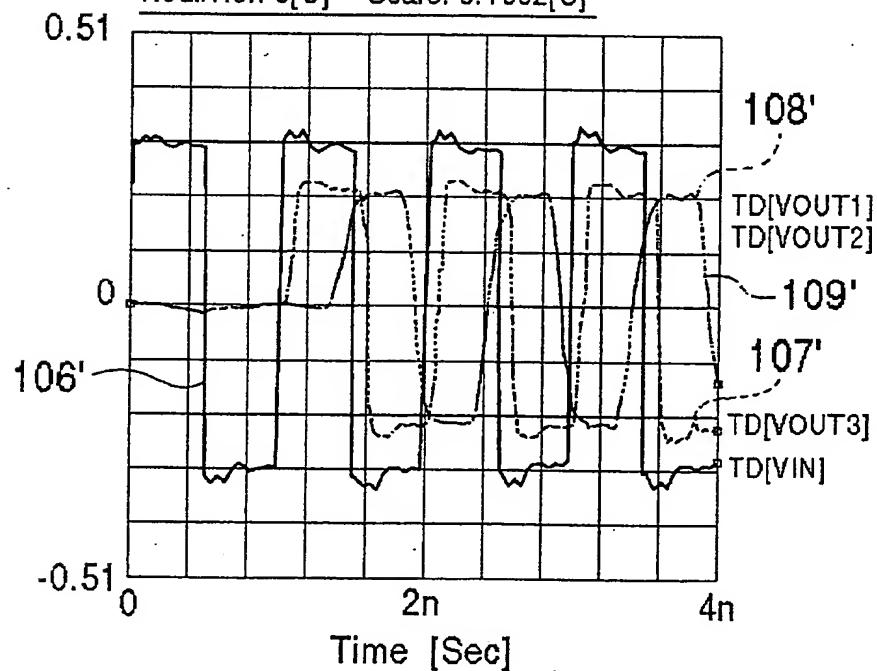


Fig. 42(a)

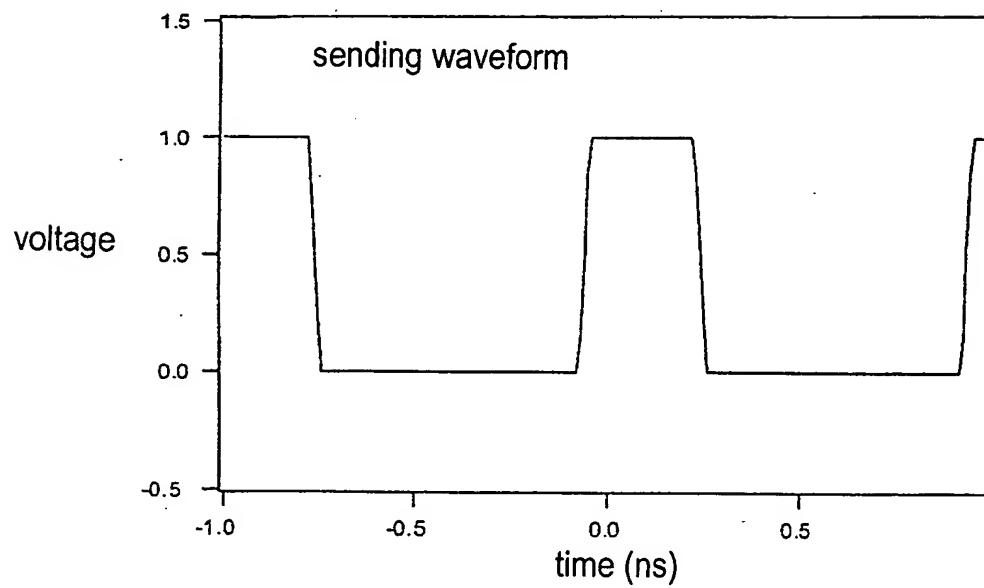


Fig. 42(b)

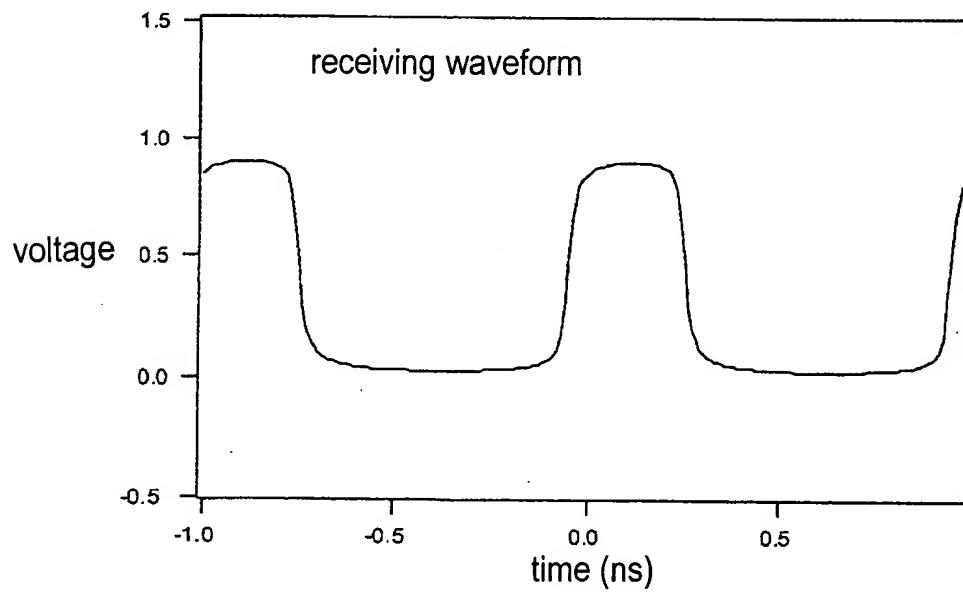
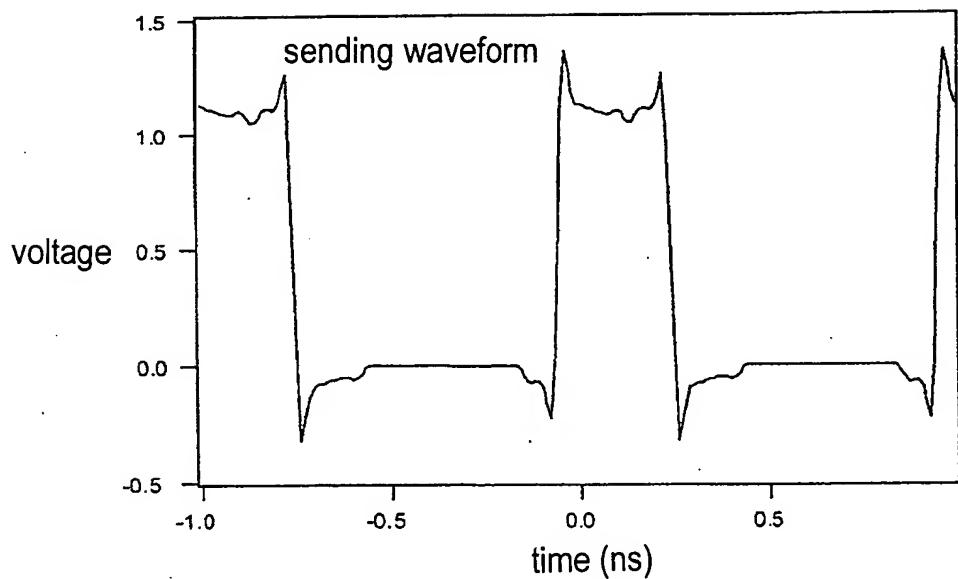


Fig. 43(a)**Fig. 43(b)**